IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 7-10, 2009

San Diego, CA

Highest Parallel Test for DRAM Enabled through Advanced TRE™

Michael Huebner

FormFactor

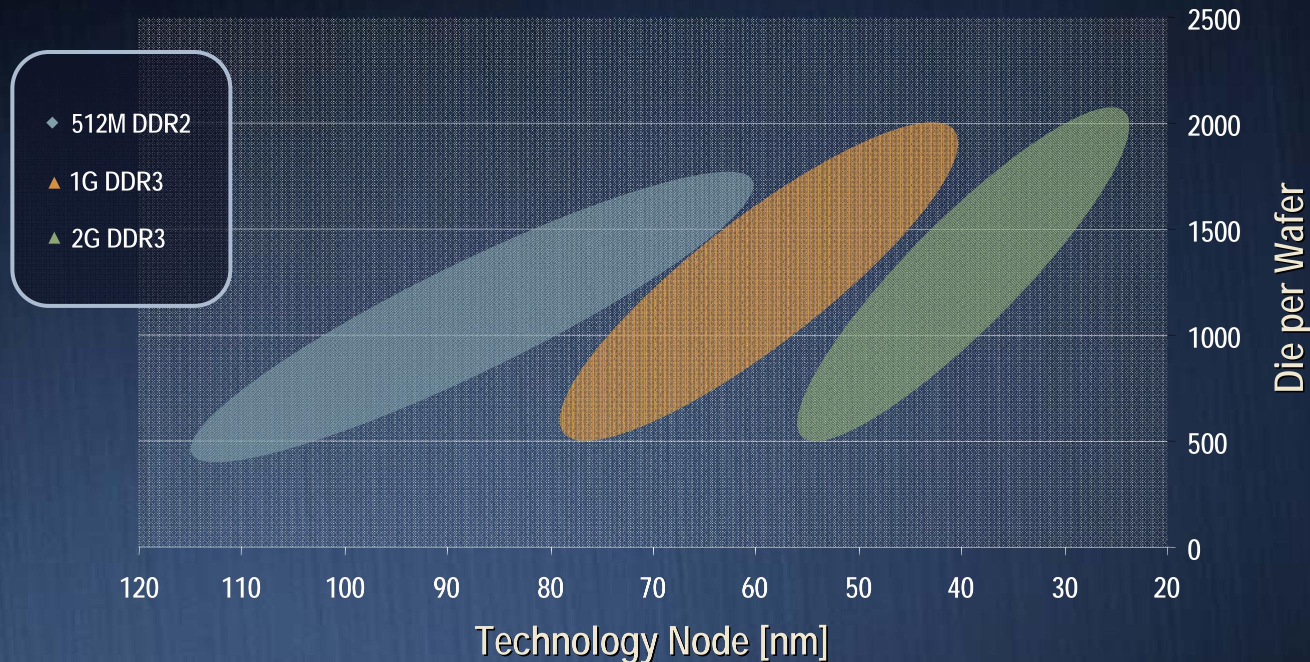
Outline

- Parallel test of DRAM
  - Die per Wafer trend
  - Probe count trend
  - Probe force
  - Parallel test methods
- Advanced TRE: Example DC-Boost™
- Vision for One Touchdown and status

Parallel Test of DRAM

- Parallel test has been a necessity for DRAM
  - Reduce test cost
  - Reduce cycle time
- Test times are long and are increasing with memory density
- Touchdown count has increased:
  - Die shrink enabled by new technology node
  - Die shrink enabled by new memory architecture ($4F^2$) – see SWTW 2008
- Increase of parallel test is the most efficient way to reduce test cost and cycle time

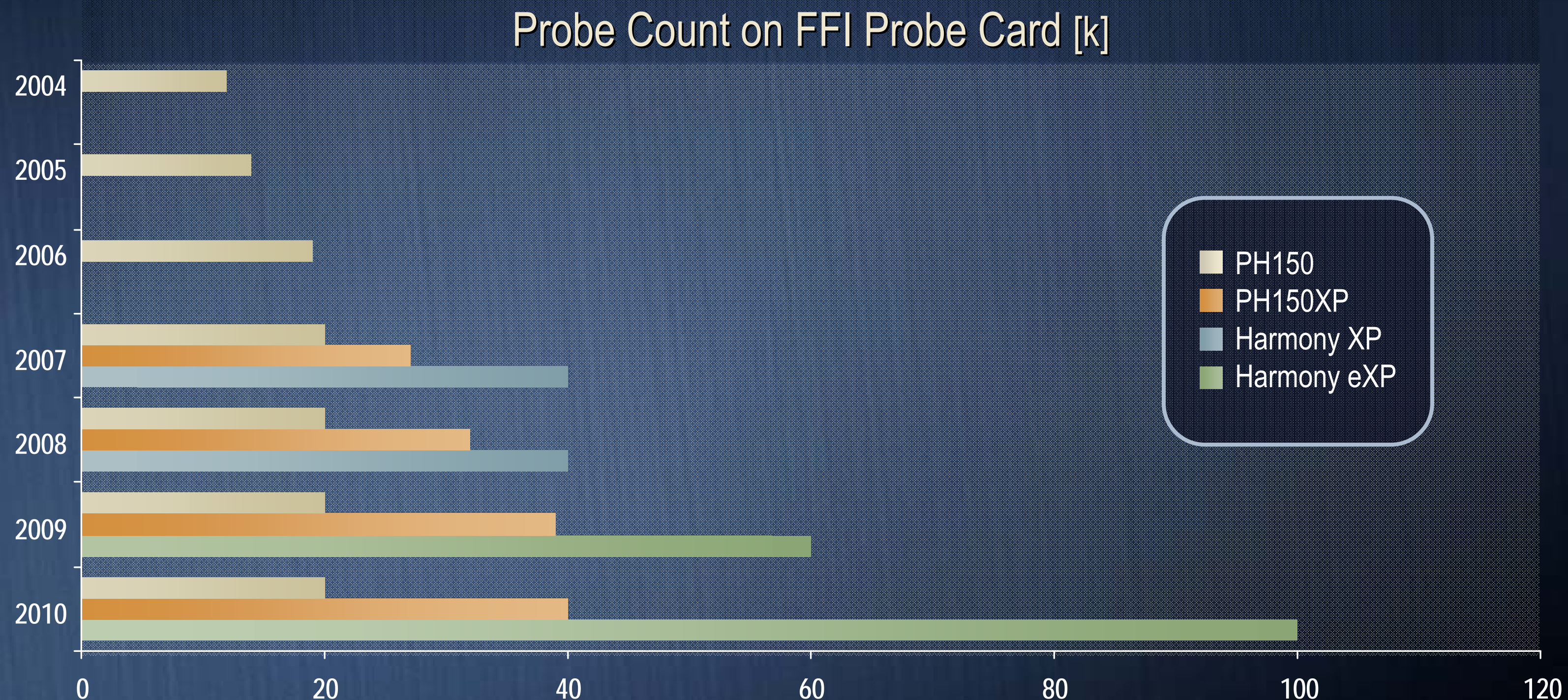
DRAM Trends – Die per Wafer and Parallelism



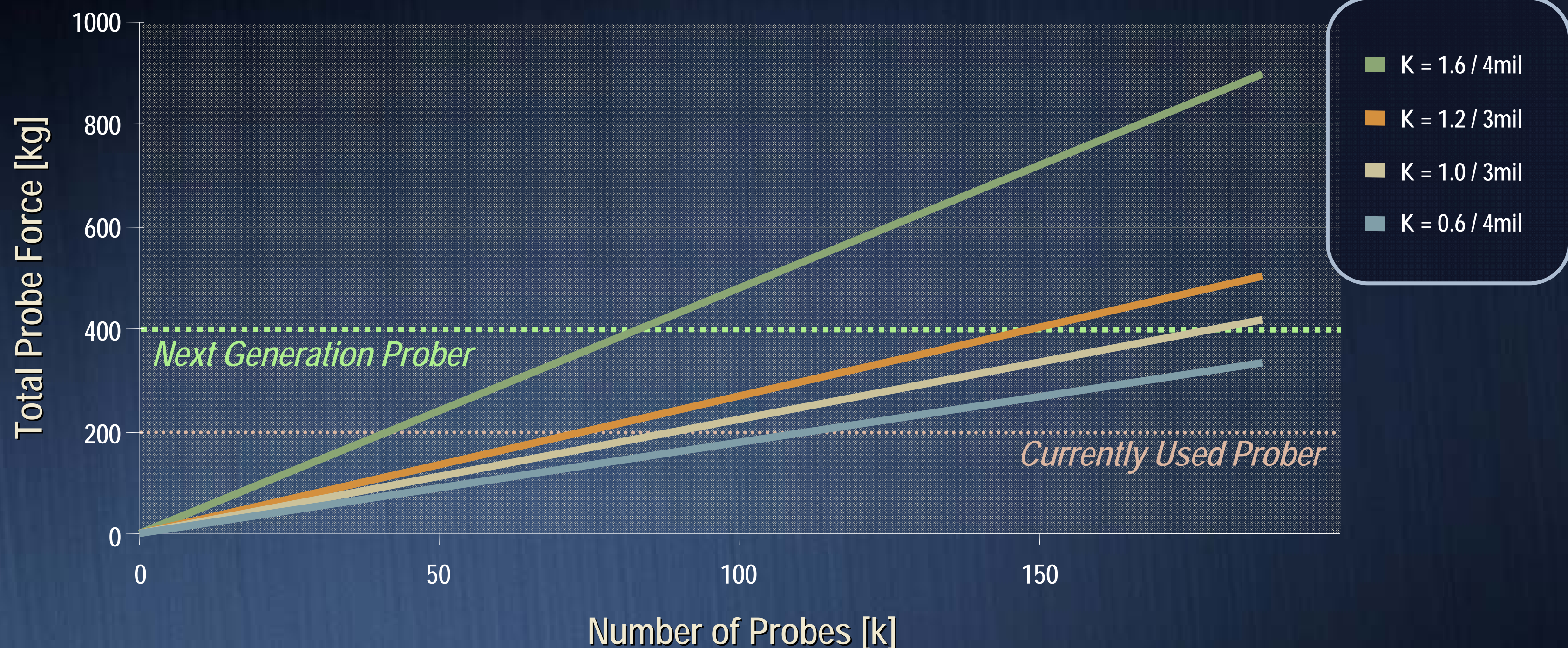
- Die per Wafer in HVM is increasing and will reach 2000 dpw with 1G DDR3
- Most 1G DDR2/3 are tested with 2 to 7 touchdowns today – depending on parallelism
- Increase in parallelism needed to reduce touchdown count

Industry Probe Count Trend 2009

- Signal count per DUT will decrease but number of power and ground probes will increase further
- Increase in parallel test will boost total probe count
- Overall probe count will continue to increase



Probe Count and Total Probe Force



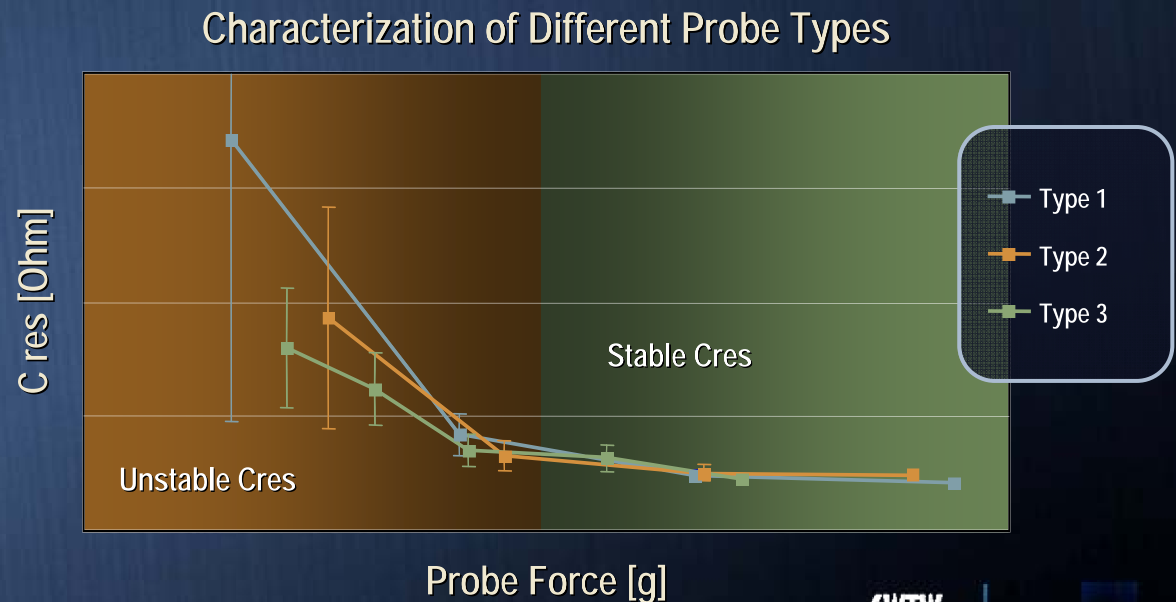
- For 1 TD or 1500 to 2000 DUT parallel test 75 to 140k probes are needed (depending on probes/DUT)
- Next generation probers are needed to support 2000 DUT
- Majority of installed probers can support ~70k probes

Challenge: Total Probe Force

- Problems arising with probe force reaching the limits of the probers:
  - System deflection (see SWTW 2008 presentations)
    - For high probe count Actual OT is only 20-60% of Programmed OT
  - Increased sensitivity to imbalanced probe layouts
    - More probes scrubbing in one direction than into the other
    - Resulting force X/Y components push the chuck
  - With higher probe count and smaller dimensions (pad size and pitch) the thermal management gets more and more important

Probe Count and Total Probe Force

- Overall probe force needs to stay in a manageable region
- Probe force per probe has to decrease
- Certain probe force is needed for stable Cres
- 3D MEMS allows to design a probe with:
  - Stable Cres
  - Enough compliance
  - Short scrub
    - Smaller pads



Parallel Test of DRAM – Past and Future

METHOD	NATIVE TEST	TRE x2 / x4 DFT		SAME + NEW TESTERS			A-TRE MORE DFT	SAME + NEW TESTER
Probes / DUT (40 / 50 / 60)		DFT			PWR + GND			
Factor	x1	x2	x4	x4	x4	x4	x8	x8
DUT	16	32	64	128	256	512	<1000	>1000
Tester Site #	16	16	16	32	64	128	64 - 128	TBD

TRE = Tester Resource Enhancement

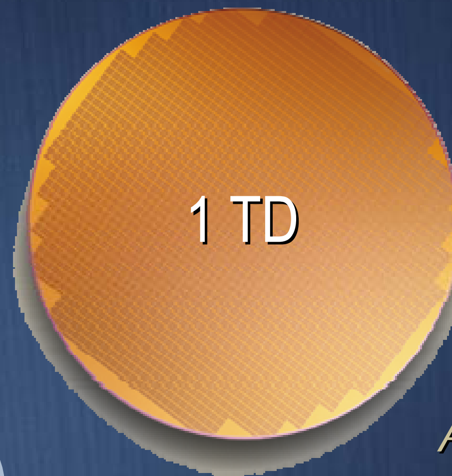
The 3 Ways to Increase Parallel Test

Massively parallel tester

- More expensive tester
- Complex probe interface
- Straight forward approach

DFT on Chip

- Simple tester and probe card
- Complex chip design
- Possible die size adder
- Time to market impact



Advanced TRE on Probe Card

- Use older less capable testers
- Flexible on new requirements
- Complex probe cards

Historically a good mix of these three methods has been most successful to increase parallel test. What will be the driver for the next step?

Advanced TRE (Tester Resource Enhancement)

- TRE in the past was limited to control signals = signal TRE
  - One tester driver controls multiple DUTs
  - Signal is split on the probe card
    - Optimized for signal integrity
- Advanced TRE is expanding TRE now to different classes of signals
- Example: DC-signals
  - DC-signals are used to force voltages - trimming
  - DC-signals are used to measure voltages - characterization
    - High accuracy is needed
  - DC-signals are more critical with regards to process related failures than control signal

More capable TRE technology is needed

DC-Boost - FFI DC-TRE Chip

Adding a new degree of intelligence to our wafer probe cards

- First custom designed TRE chip
- Enables TRE on DC-signals:
  - One tester channel can be used for multiple DC-signals
  - Sequence control is provided for voltage measurements
    - Allow sequential measurements by connecting one signal at a time
  - Isolation capability is provided for disconnecting bad DUTs
    - Minimize yield loss
    - Increase accuracy of applied voltage levels

DC-Boost - FFI DC-TRE Chip

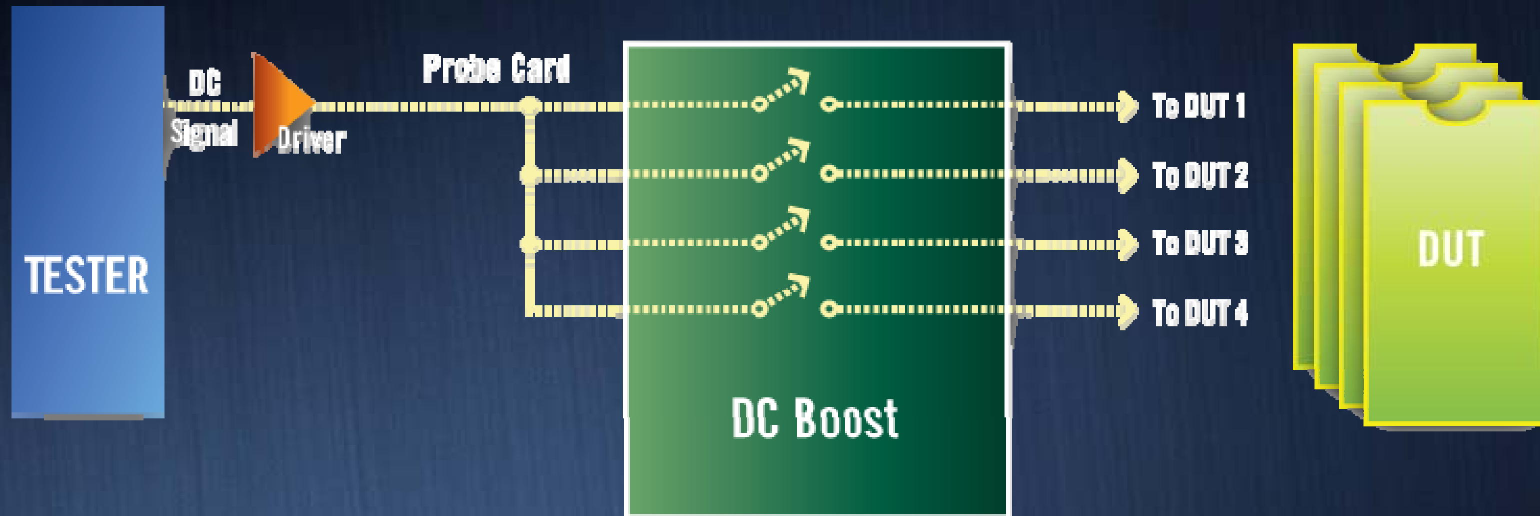
Adding a new degree of intelligence to our wafer probe cards

Advantages

- Extend parallel test
  - Double parallelism in combination with other TRE and DFT
  - Extend the life of older tester platforms
- Allow increase of DC-signals per DUT
  - Trend to increase number DC-signals
    - Provides better test coverage
    - New technology nodes tend to need more DC-signals
    - DC-Boost can enable more DC-signals on older tester platforms
    - Flexibility to react on changing device requirements

DC-Boost - FFI DC-TRE Chip

Adding a new degree of intelligence to our wafer probe cards

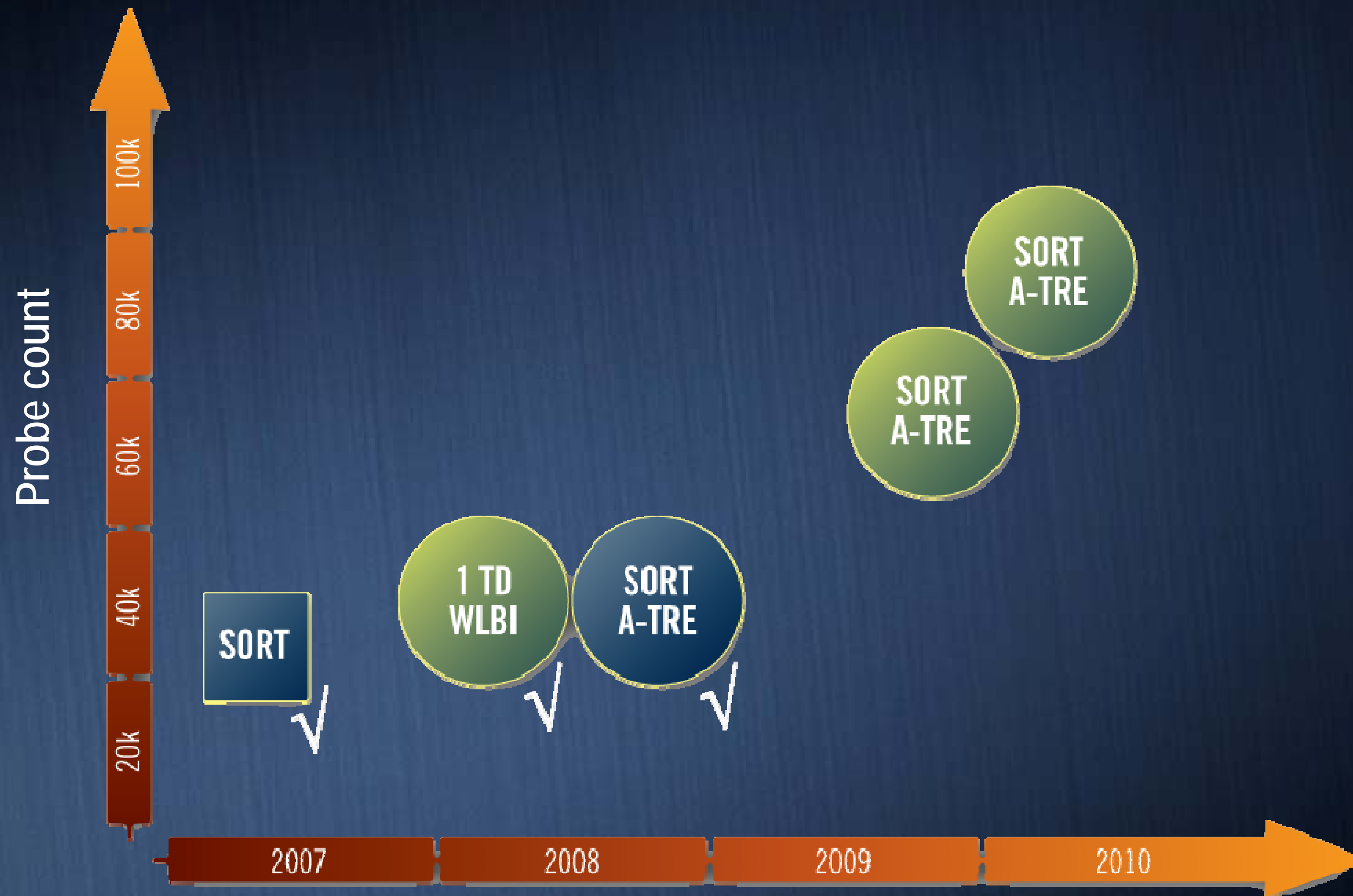


- Smaller than other alternative solutions – need 2 to 5k switches today
- Wide temperature range to support high temp SORT and WLBI
- Isolation capability – up to 8 DUT use the same driver
- Smart control interface – many switches need to be controlled

DC-Boost - Results

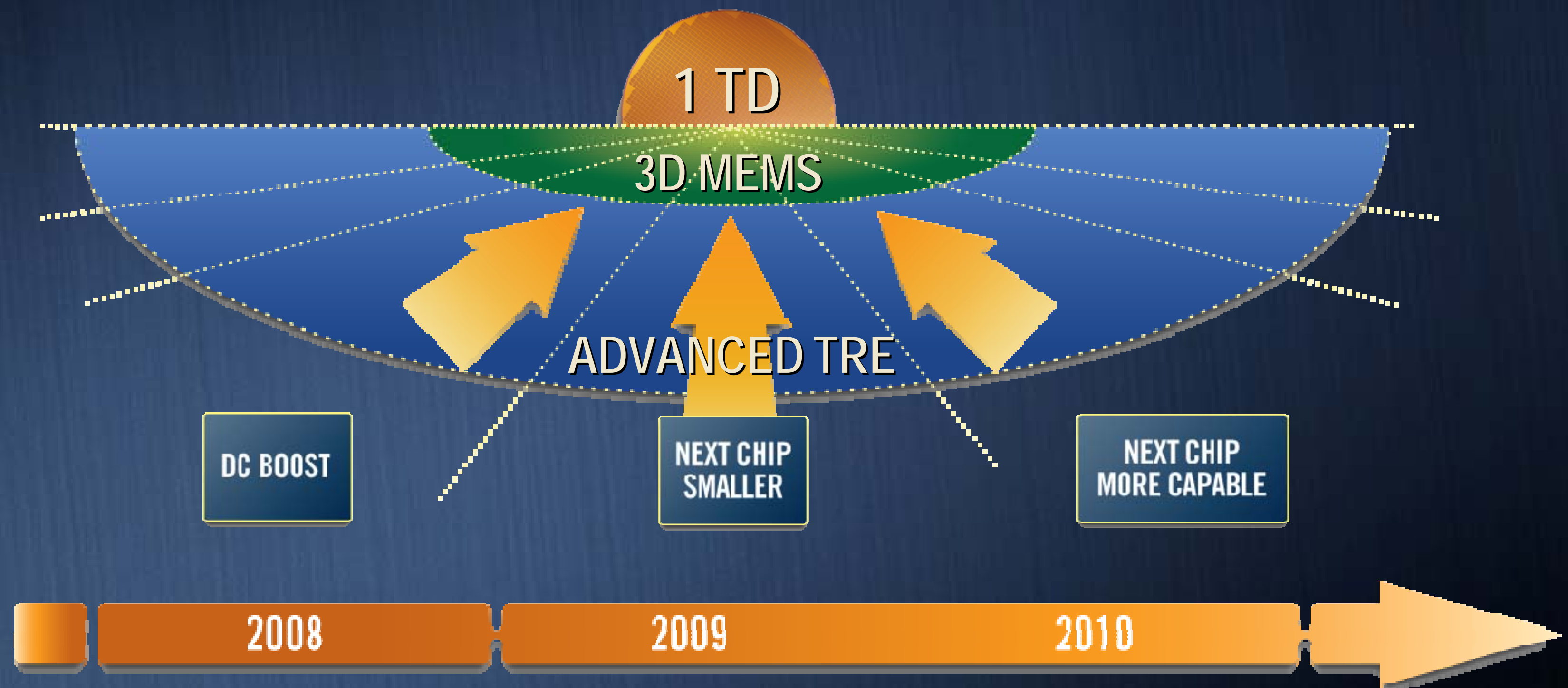
- Built several probe cards using DC-Boost
- Running in production at multiple customer sites
- Perfect correlation with non DC-TRE case
- No yield impact compared to non DC-TRE case

Milestones on the Road to 1 TD DRAM SORT



One Touchdown Vision

- Extend test capability via integrated IC development
- Use 3D MEMS probes to enable high probe count probe cards



Acknowledgements

Special thanks to:

- FFI Advanced TRE engineering team
- FFI Application and Product Solution Team